WHAT IS CLAIMED IS:

1. A video signal processing circuit that samples an analog composite video signal, converts the composite video signal to a digital signal, and processes the composite video signal by using a prescribed clock signal, comprising:

a clock generating means generating the prescribed clock signal;

a phase detecting means detecting color subcarrier phase information in each line of the composite video signal;

a phase difference calculation means calculating a phase difference between phase information obtained from the phase detecting means and a prescribed reference phase, calculating a phase correction from the phase difference, and outputting the phase correction;

a sampling phase conversion means correcting the phase at which the composite video signal is sampled according to the phase correction output from the phase difference calculation means; and

a luminance/chrominance (Y/C) separation means separating a luminance signal and a chrominance signal from the composite video signal output from the sampling phase conversion means.

2. The video signal processing circuit of claim 1, wherein the phase detecting means detects a burst phase in each line of the composite video signal and outputs the burst phase as the color subcarrier phase information of the line.

3. The video signal processing circuit of claim 1, further comprising a color demodulating means demodulating the chrominance signal separated by the Y/C separation means according to a color subcarrier reference signal to obtain color difference signals, wherein:

the phase detecting means detects the burst phase in each line of the composite video signal, outputs the burst phase as the color subcarrier phase information of the line, and generates the color subcarrier reference signal according to the detected burst phase.

4. The video signal processing circuit of claim 1, wherein the prescribed reference phase is the reference phase of a target line determined by a prescribed fixed phase value and the phase information of the target line; and

the phase difference calculation means calculates a phase difference between the phase information of a certain line and the reference phase of the target line, the certain line being separated by a prescribed number of lines or fields from the target line.

5. The video signal processing circuit of claim 4, wherein the phase difference calculation means comprises:

a delaying means applying a delay of the prescribed number of lines or fields to the phase information from the phase detecting means;

a phase error calculation means obtaining a phase difference between the phase information of the certain line and the reference phase of the target line, including phase information of the target line, as a phase error; and

a correction conversion means converting the phase error to a phase correction with reference to one period of the clock generated by the clock generating means.

6. The video signal processing circuit of claim 1, wherein the prescribed reference phase includes a fixed phase value predetermined by the line position of the composite video signal; and

the phase difference calculation means calculates a

phase difference between the phase information and the fixed reference phase.

7. The video signal processing circuit of claim 6, wherein the phase difference calculation means comprises:

a delaying means applying a delay of the prescribed number of lines or fields to the phase information from the phase detecting means;

a phase error calculation means obtaining both a phase difference between the phase information of the target line and the fixed reference phase and a phase difference between the phase information of the certain line separated by a prescribed number of lines or fields from the target line and the fixed reference phase as phase errors; and

a correction conversion means converting the phase error to a phase correction with reference to one period of the clock.

8. The video signal processing circuit of claim 6, wherein the phase difference calculation means comprises:

a phase error calculation means obtaining a phase difference between the phase information from the phase detecting means and the fixed reference phase as a phase error; and

a correction conversion means converting the phase error to a phase correction with reference to one period of the clock.

9. The video signal processing circuit of claim 1, wherein the sampling phase conversion means comprises:

a delaying means applying a delay of a prescribed number of lines or fields to the composite video signal; and

a phase correction means correcting the phase at which the composite video signal of a certain line separated by a

prescribed lines or fields from the target line, or the composite video signal of the target line and the composite video signal of the prescribed line, is sampled, in accordance with the output from the phase difference calculation means.

10. The video signal processing circuit of claim 9, wherein the phase correction means comprises:

a coefficient generating means generating coefficients of a filter having a group delay corresponding to the output from the phase difference calculation means; and

a filter means performing filtering of the composite video signal in accordance with the coefficients.

11. The video signal processing circuit of claim 9, wherein the phase correction means comprises:

a plurality of delaying means applying a certain delay to the composite video signal; and

a selection means selecting the output of the plurality of delaying means in accordance with the output from the phase difference calculation means.

12. The video signal processing circuit of claim 9, wherein the phase correction means comprises:

a coefficient generating means generating an interpolation filter coefficient for obtaining the value of a point corresponding to a position offset from the sampling position of the composite video signal by the phase difference corresponding to the output of the phase difference calculation means; and

a filter means performing filtering of the composite video signal in accordance with the coefficient.

13. The video signal processing circuit of claim 1, further

comprising:

an A/D conversion means converting the input analog composite video signal to a digital composite video signal,

the sampling phase conversion means comprising:

a clock phase correction means correcting the phase of the clock generated by the clock generating means in accordance with the output from the phase difference calculation means; and

a delaying means applying a delay of a prescribed number of lines or fields to the digitized composite video signal;

wherein the A/D conversion means converts the composite video signal to a digital signal by using a clock with a phase corrected by the clock phase correction means.

14. The video signal processing circuit of claim 1, wherein the Y/C separation means separates the luminance signal and the chrominance signal from the composite video signal by means of a line comb filter or frame comb filter, by using the composite video signal output from the sampling phase conversion means in a plurality of lines.

15. The video signal processing circuit of claim 1, wherein the clock generating means generates a clock signal with a frequency equal to an integer multiple of 13.5 MHz, regardless of the television broadcast system of the composite video signal, for the processing of the composite video signal.

16. The video signal processing circuit of claim 1, wherein the clock generating means generates a burst locked clock in phase with the burst signal in the composite video signal for the processing of the composite video signal.

17. The video signal processing circuit of claim 1, wherein

the clock generating means generates a line locked clock in phase with the horizontal sync signal in the composite video signal for the processing of the composite video signal.

18. The video signal processing circuit of claim 1, further comprising a television broadcast system setting means specifying a broadcast system of the composite video signal, wherein:

the phase detecting means detects a color subcarrier phase in accordance with the broadcast system specified by the television broadcast system setting means;

the phase difference calculation means obtains the phase difference in accordance with the specified television broadcast system; and

the Y/C separation means separates the luminance signal and the chrominance signal from the composite video signal in accordance with the specified television broadcast system.

19. A video signal display device comprising the video signal processing circuit of claim 1.

20. A video signal recording device comprising the video signal processing circuit of claim 1.